

# DATA SHEET

**TDA8575**

**Ground noise isolation amplifier**

Preliminary specification  
File under Integrated Circuits, IC01

1996 Jul 29

## Ground noise isolation amplifier

## TDA8575

## FEATURES

- High common mode rejection up to high frequencies
- Reduced dependency of common mode rejection on source resistance
- Low distortion
- Low noise
- AC and DC short-circuit safe
- Few external components
- ESD protected on all pins.

## GENERAL DESCRIPTION

The TDA8575(T) is a two channel amplifier with differential input and single-ended output for use in car audio applications. The differential amplifier has a gain of 0 dB, a low distortion and a high common mode rejection. The TDA8575T comes in a 16 pin SO package and TDA8575 comes in a 16 pin DIP package.

The TDA8575(T) is developed for those car audio applications where long connections between signal sources and amplifiers (or boosters) are necessary and ground noise has to be eliminated.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC}$	supply voltage		5	8.5	18	V
$I_{CC}$	supply current	$V_{CC} = 8.5\text{ V}$	–	12.6	15	mA
$G_v$	voltage gain		–0.5	0	+0.5	dB
$V_{o(rms)(max)}$	maximum output voltage (RMS value)	THD = 0.1%	–	1.7	–	V
SVRR	supply voltage ripple rejection		55	60	–	dB
CMRR	common mode rejection ratio	$R_s = 0\ \Omega$	–	80	–	dB
THD	total harmonic distortion	$V_{o(rms)} = 1\text{ V}; f = 1\text{ kHz}$	–	0.005	–	%
$V_{no}$	noise output voltage		–	3.7	5	$\mu\text{V}$
$ Z_i $	input impedance		–	108	–	$\text{k}\Omega$
$ Z_o $	output impedance		–	–	10	$\Omega$

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8575T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TDA8575	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1

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BLOCK DIAGRAM

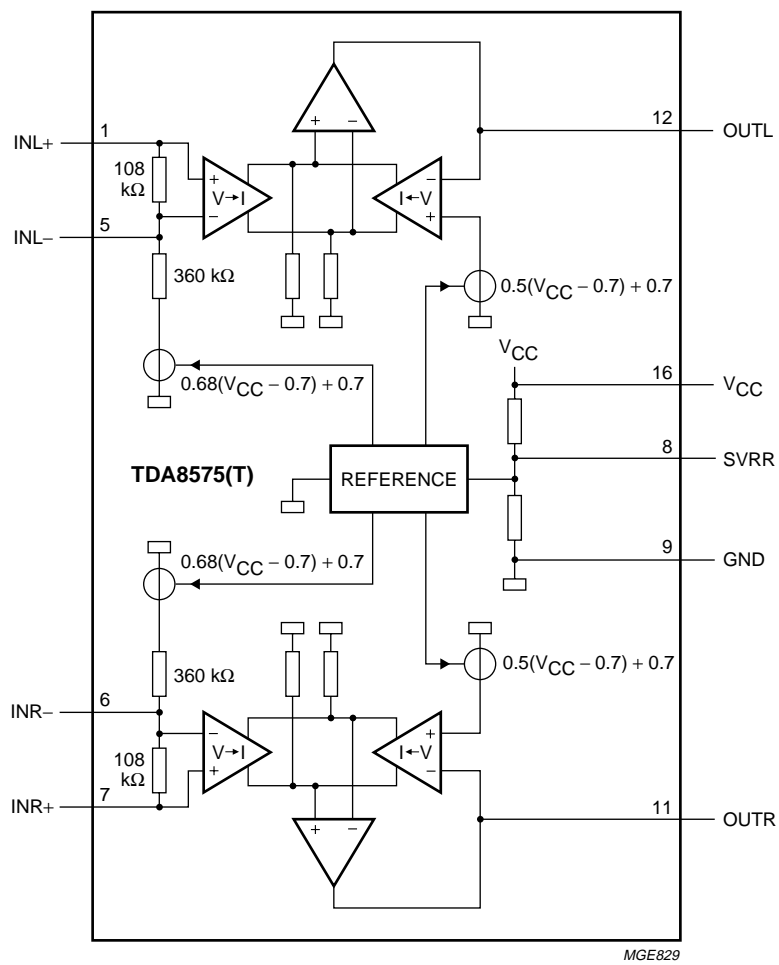


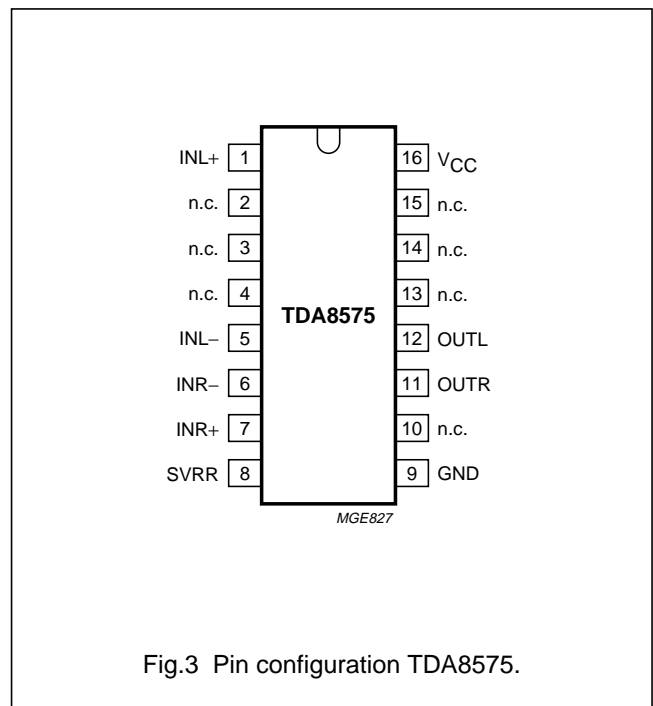
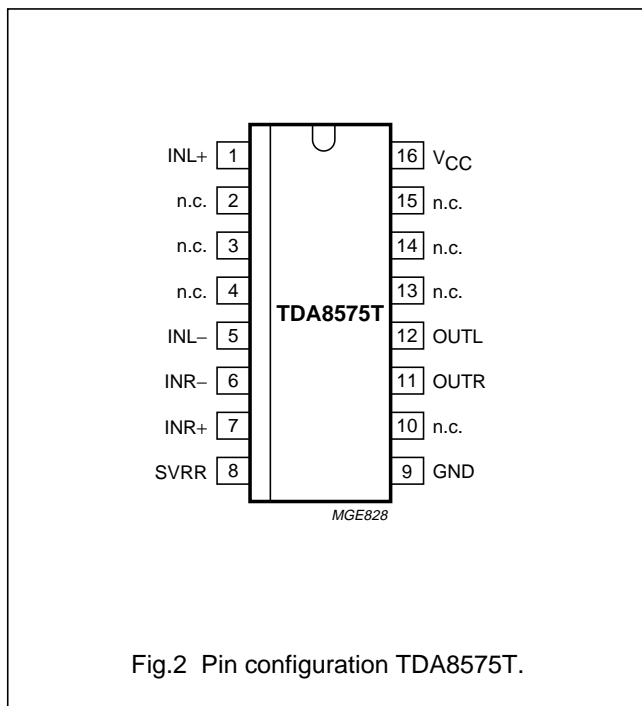
Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
INL+	1	positive input left
n.c.	2	not connected
n.c.	3	not connected
n.c.	4	not connected
INL-	5	negative input left
INR-	6	negative input right
INR+	7	positive input right
SVRR	8	supply voltage ripple rejection
GND	9	ground
n.c.	10	not connected
OUTR	11	output voltage right channel
OUTL	12	output voltage left channel
n.c.	13	not connected
n.c.	14	not connected
n.c.	15	not connected
V <sub>CC</sub>	16	supply voltage



# Ground noise isolation amplifier

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## FUNCTIONAL DESCRIPTION

### System description

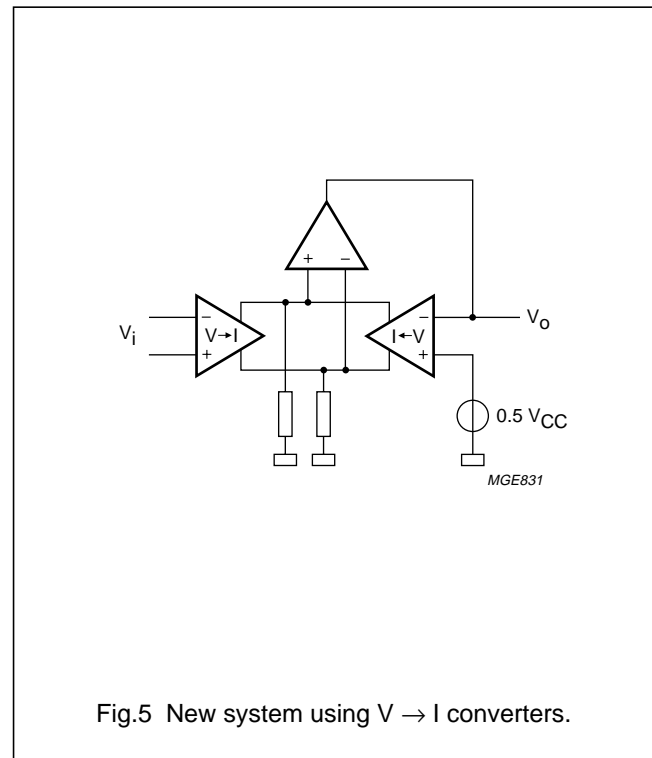
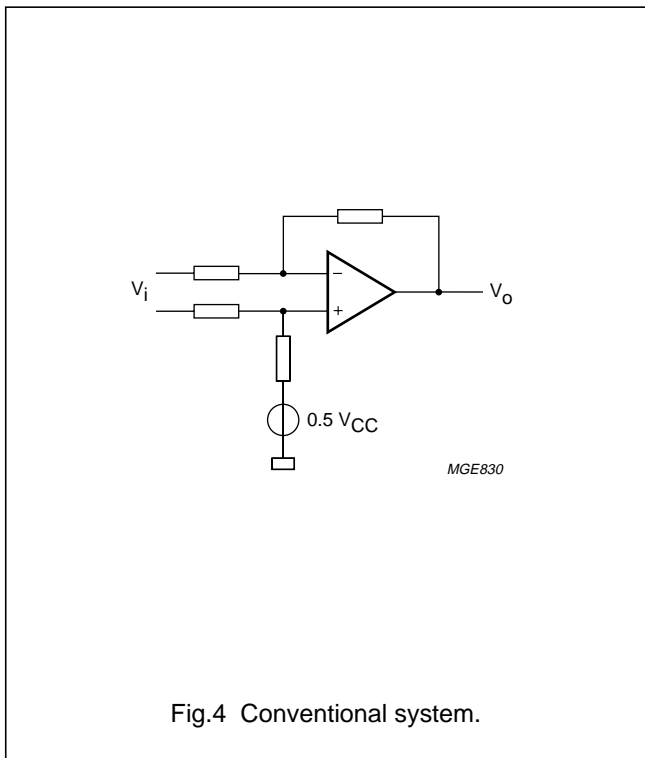
To enable a high common mode rejection a new system setup is used. The voltage to current converter, referred to as  $V \rightarrow I$  in the block diagram of Fig.1, replaces the resistors that can be seen in the conventional system solution.

Both systems are shown in Figs 4 and 5. In the conventional system the common mode rejection is limited by the matching properties of the resistors resulting in a CMRR of 60 dB maximum. Using the new system setup a CMRR of 80 dB is achieved.

### Power on

In Fig.6 the preferred input capacitor values are shown. If the capacitor  $C2 = 22 \mu F$  connected to the IN- inputs had to be charged by the  $0.5V_{CC}$  voltage source a charge time of  $5\tau = 5 \times \frac{360 \text{ k}\Omega}{2} \times 22 \mu F = 20 \text{ s}$  would be required.

This is inconvenient for most applications and therefore the TDA8575(T) is equipped with a quick charge circuit. On power-on the quick charge circuit charges the capacitor C2 connected to the IN- pins. The quick charge circuit consists of a voltage buffer and a control circuit (referred to as 'reference and power check' in Fig.6) that monitors the supply voltage  $V_{CC}$ . If the supply voltage rises more than  $\approx 2 \text{ V}$  the voltage buffer is switched on. After charging C2 the voltage buffer is switched off. The charge time of C2 will equal the charge time of C4, the SVRR capacitor.



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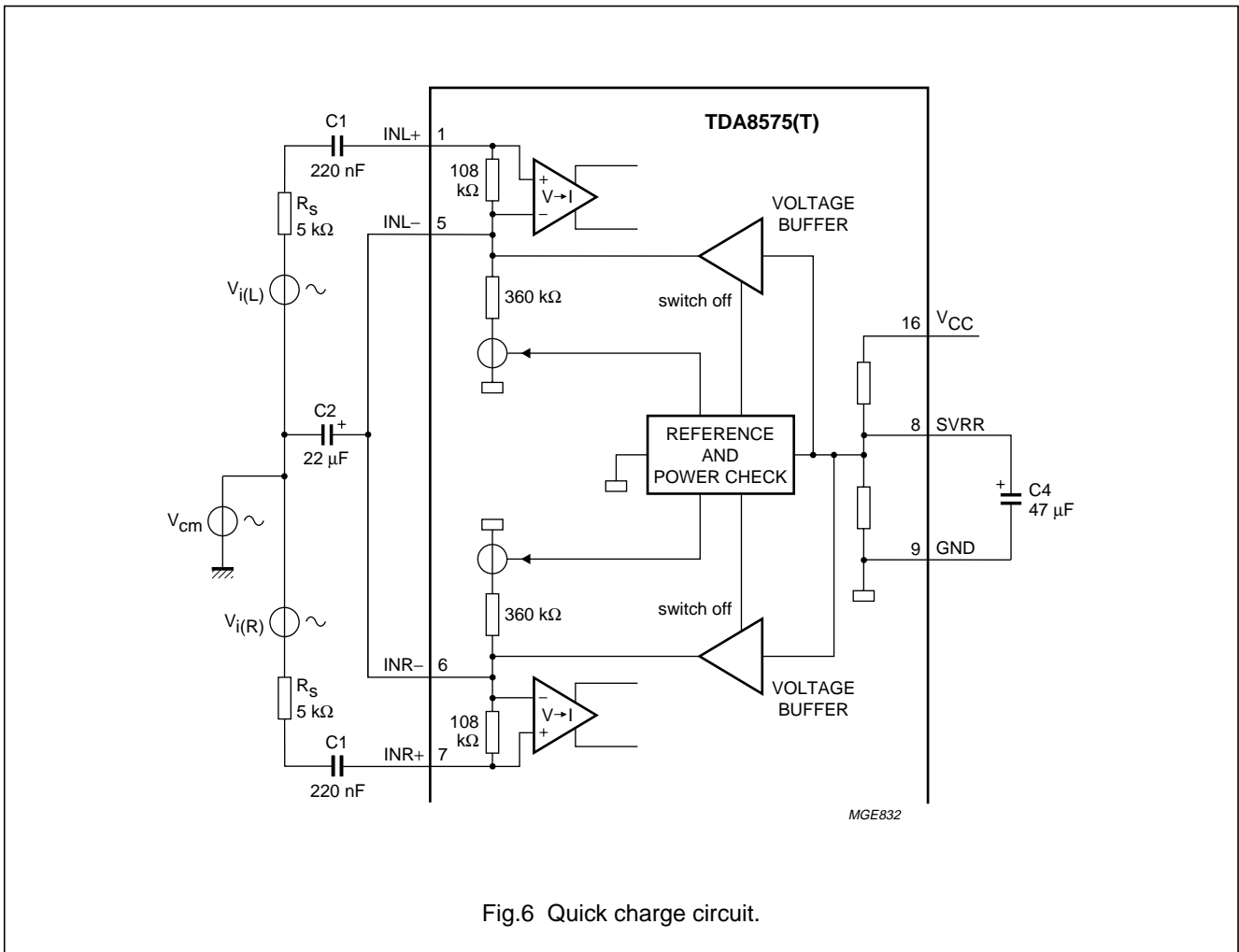


Fig.6 Quick charge circuit.

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage	operating	–	18	V
$I_{ORM}$	repetitive peak output current		–	40	mA
$V_{sc}$	AC and DC short-circuit safe voltage		–	18	V
$T_{stg}$	storage temperature		–55	+150	°C
$T_{amb}$	operating ambient temperature		–40	+85	°C
$T_j$	junction temperature		–	+150	°C

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air		
	TDA8575 (DIP16)	75	K/W
	TDA8575T (SO16)	110	K/W

**QUALITY SPECIFICATION**

Quality according to *UZW-BO/FQ-0601*, if this type is used as an audio amplifier.

**DC CHARACTERISTICS**

$V_{CC} = 8.5\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $R_L = 10\text{ k}\Omega$ ; in accordance with application circuit (see Fig.9).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC}$	supply voltage	$V_i = 0\text{ V}$	5	8.5	18	V
$I_{CC}$	supply current		–	12.6	15	mA
$V_O$	output voltage	note 1	–	4.7	–	V

**Note**

1. The DC output voltage with respect to ground is approximately  $0.5V_{CC}$ .

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**AC CHARACTERISTICS** $V_{CC} = 8.5 \text{ V}$ ;  $f = 1 \text{ kHz}$ ;  $R_S = 0 \text{ k}\Omega$ ;  $R_L = 10 \text{ k}\Omega$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; in accordance with application circuit (see Fig.9).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$G_V$	voltage gain		-0.5	0	+0.5	dB
$\alpha_{cs}$	channel separation	$R_S = 5 \text{ k}\Omega$ ; note 1	70	80	-	dB
$ \Delta G_V $	channel unbalance		-	-	0.5	dB
$f_{ro(L)}$	low frequency roll-off	-1 dB; note 2	-	-	20	Hz
$f_{ro(H)}$	high frequency roll-off	-1 dB	20	-	-	kHz
$ Z_i $	input impedance		80	108	123	k $\Omega$
$ Z_o $	output impedance		-	-	10	$\Omega$
$V_{i(rms)(max)}$	maximum input voltage (RMS value)	THD = 1%	-	1.7	-	V
$V_{no}$	noise output voltage	unweighted; note 3	-	3.7	5	$\mu\text{V}$
THD	total harmonic distortion	$V_{i(rms)} = 1 \text{ V}$	-	0.005	0.01	%
		$V_{i(rms)} = 1 \text{ V}$ ; $f = 20 \text{ Hz to } 20 \text{ kHz}$	-	0.01	-	%
THD <sub>max</sub>	total harmonic distortion at maximum output current	$V_{i(rms)} = 1 \text{ V}$ ; $R_L = 150 \text{ }\Omega$	-	-	1	%
$V_{i(cm)(rms)}$	common-mode input voltage (RMS value)		-	-	1	V
CMRR	common-mode rejection ratio	$R_S = 5 \text{ k}\Omega$	66	80	-	dB
		$R_S = 0 \text{ }\Omega$ ; note 4 $f = 100 \text{ Hz to } 20 \text{ kHz}$	-	80	-	dB
SVRR	supply voltage ripple rejection	$R_S = 2 \text{ k}\Omega$ ; note 5	55	-	-	dB
		$R_S = 2 \text{ k}\Omega$ ; note 5 $f = 20 \text{ Hz to } 20 \text{ kHz}$	-	60	-	dB

**Notes**

1. The channel separation is dependent on the capacitor C2 connected to the IN- input. The channel separation for low frequencies (<1 kHz) can be increased by using a larger capacitance for C2.
2. The frequency response is externally fixed by the input and output coupling capacitors.
3. The noise output voltage is measured in a bandwidth of 20 Hz up to 20 kHz, unweighted.
4. The common mode rejection ratio is measured at the output with a voltage source  $V_{cm(rms)} = 1 \text{ V}$  and both  $V_{i(L)}$  and  $V_{i(R)}$  short-circuited according to Fig.9. The common mode rejection is dependent on the capacitor C2 connected to the IN- input. The common mode rejection for low frequencies (<1 kHz) can be increased by using a larger capacitance for C2.
5. Supply voltage ripple rejection is measured at the output using a ripple amplitude of 2 V (p-p). The source resistance  $R_S = 2 \text{ k}\Omega$ .



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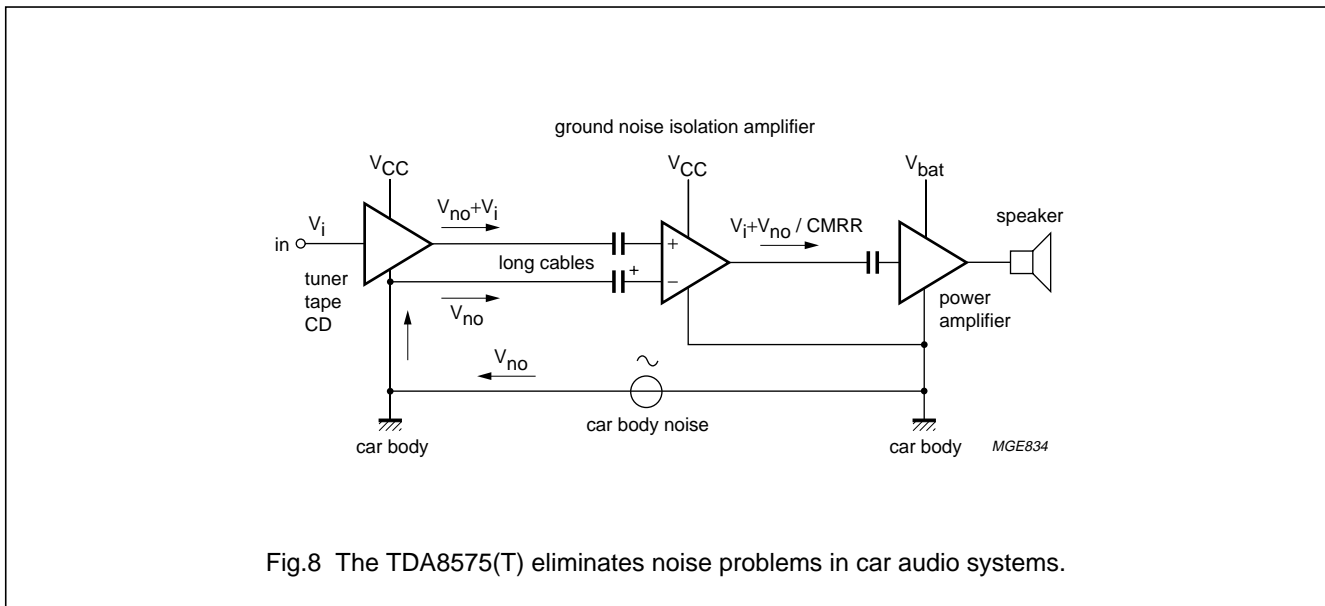
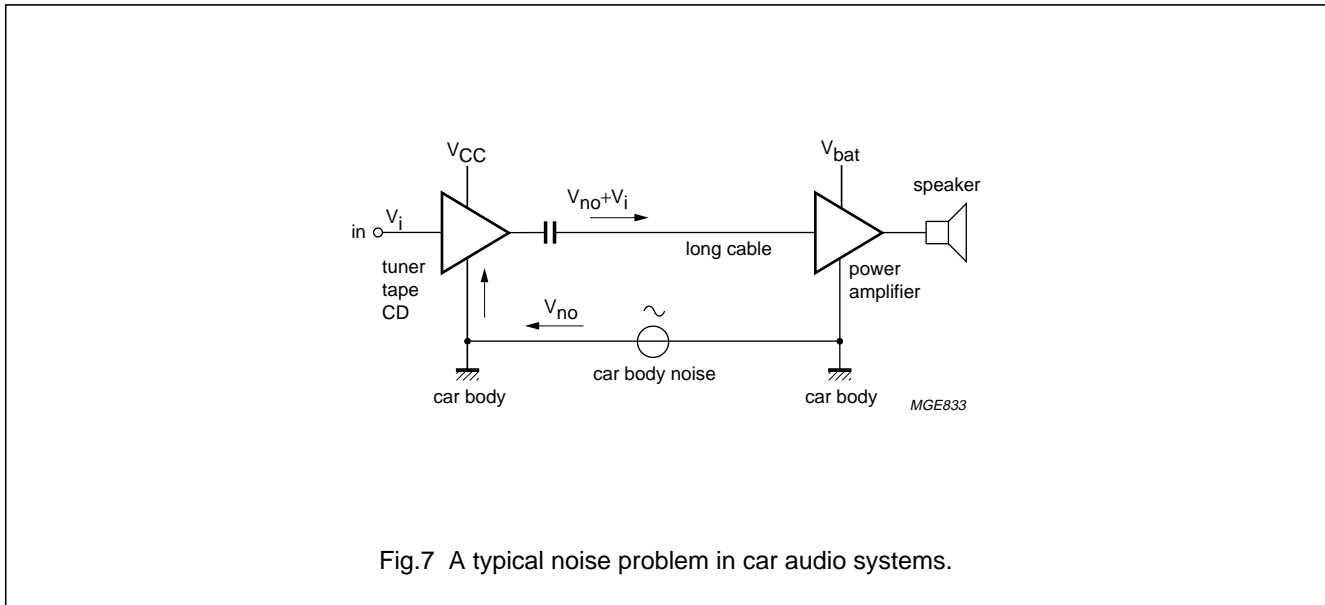
# TDA8575

## APPLICATION INFORMATION

### General

The TDA8575(T) is a two channel amplifier with differential input and single-ended output for use in car audio applications. The differential amplifier has a gain of 0 dB, a low distortion and a high common mode rejection.

Due to wiring resistance and noise coming from various electric devices in the automobile, performance loss will appear in those car audio applications where long connections between signal sources and amplifiers (or boosters) are necessary. To solve these problems the TDA8575(T) is developed (see Figs 7 and 8).



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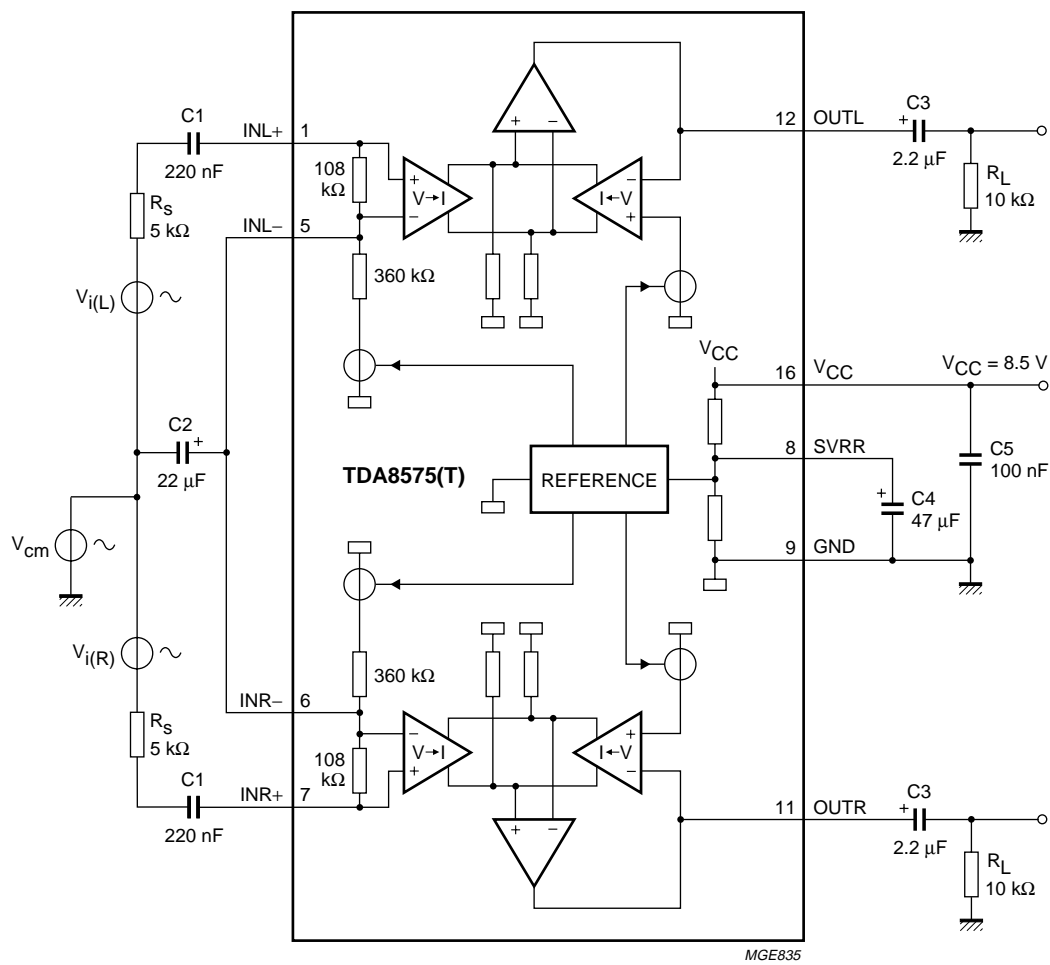


Fig.9 Application circuit TDA8575(T).

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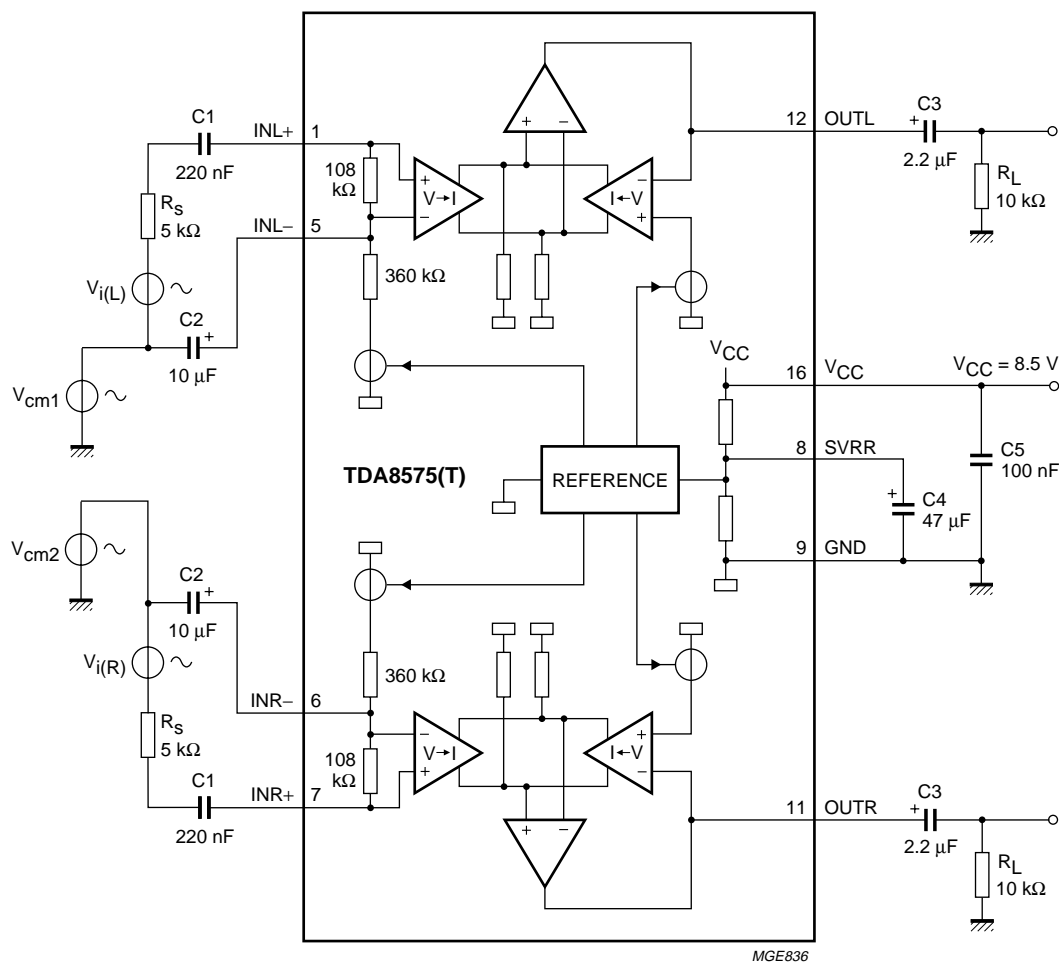


Fig.10 Application circuit TDA8575(T) with a balanced signal source.

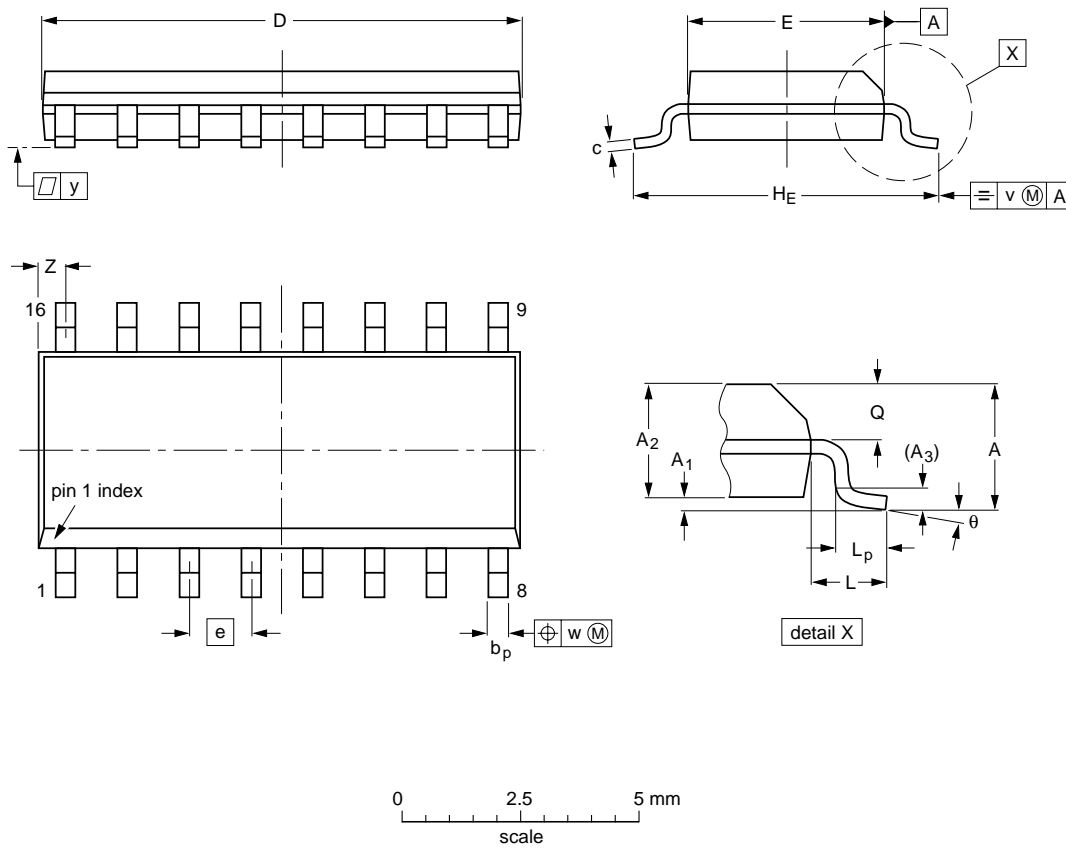
Ground noise isolation amplifier

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PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

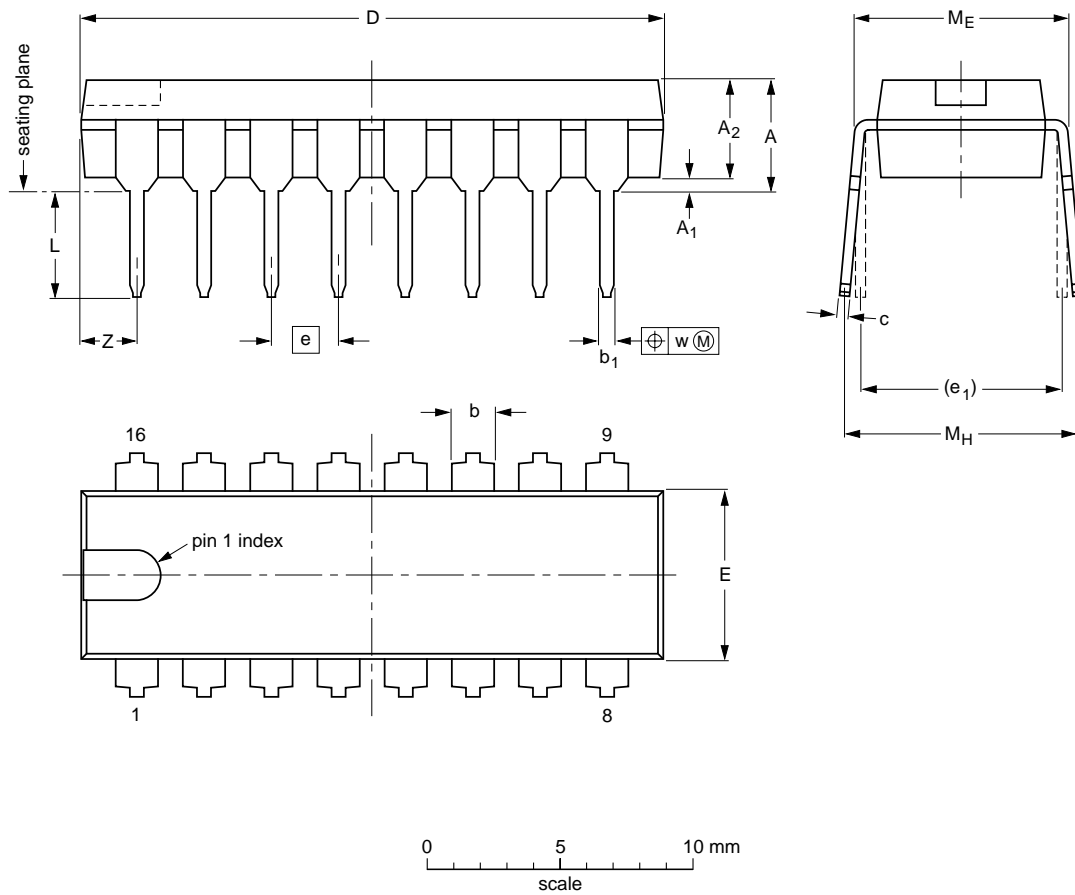
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

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DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				92-10-02 95-01-19

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

#### DIP

##### SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### SO

##### REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

##### WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

##### REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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